REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 and 29-31 are presently active in this case, Claims 1-3, 5-12 and 15 amended, and Claims 29-31 added by the present amendment. Claims 16-28 were previously withdrawn from consideration.

In the outstanding Official Action the title was objected to as not being descriptive; Claims 7-9 and 12 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which appl9icant regards as the invention; Claims 1-2 and 10-13 were rejected under 35 USC §102(a) as being anticipated by Leobandung et al (6,180,486); Claims 1, 3, 4 and 6 were rejected under 35 USC §102(a) as being anticipated by Chen et al (6,214,653); Claim 15 was rejected under 35 USC §103(a) as being unpatentable over Leobandung et al in view of Sato et al 200 symposium on VLSI Technology Digest, pages 82-83 (13 June 2000); Claims 7-9 wee indicated as being allowable if rewritten to overcome the rejection under 35 USC §112, set forth; and Claims 5 and 14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

In response to the objection to the title, a new title, SEMICONDUCTOR CHIP WHICH COMBINES BULK AND SOI REGIONS AND SEPARATES SAME WITH PLURAL ISOLATION REGIONS, similar to that suggested by the Examiner and consistent with the claimed invention, has been adopted herewith.

Applicants acknowledge with appreciation the indication that Claims 7-9 and 12 include allowable subject matter. In response to this indication and in response to the rejection of Claims 7-9 and 12 as being indefinite, Claims 7-9 and 12 have been amended to

be in independent form and to clarify the claimed invention, without the addition of new matter. The amendments to Claims 7-9 and 12 are clarifying of the claimed invention, while maintaining the original scope, and are believed to place these claims in compliance with 35 USC §112, second paragraph. In view of the indication of allowable subject matter, Claims 7-9 and 12 are believed to be in condition for allowance.

New Claims 29-31 have also been added by the present amendment. Support for new Claim 29 is found in the original specification at page 10 line 2 – line 9, and Fig. 2; for Claim 30 at page 32 line 5 – page 33 line 5; and for Claim 31 at page 32 line 9 – page 33 line 5. Accordingly, no new matter has been added.

In response to the rejection under 35 U.S.C. 102(a), Claim 1 has been amended to recite the first and second isolations formerly recited in Claim 3, and thus no new matter has been added. This structure is believed to be patentably distinguishing for the reasons next discussed.

Briefly recapitulating, Applicant's invention is directed to a semiconductor chip having a functional block positioned in an SOI region and another functional block positioned in a bulk region in a single chip. To that end, the claimed semiconductor chip comprises a base substrate; a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer; a first isolation formed in the bulk device region so as to separate the bulk device; an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; a second isolation in the SOI device region so as to separate the SOI device;

and a boundary layer located at a boundary between the bulk device region and the SOI device region.

Aeeording to the elaimed invention, the semieonductor chip can eliminate the stress between the bulk region and the SOI substrate region without increasing chip size, and which allows the circuit elements to be positioned at a uniform level.

Leobandung et al. diselose a planar SOI strueture, but provide no diselosure or suggestion of the claimed first isolation formed in the bulk device region so as to separate the bulk deviee and second isolation formed in the SOI deviee region so as to separate the SOI device. Although, FIG. 8 of Leobandung et al. shows a planar SOI structure having an oxide region 36 which isolates the non-SOI area 38 from the active SOI area 40 of the SOI substrate (see column 5, line 20-31), Leobandung et al. fail to show claimed first and second isolations. Furthermore, it is evident that the treneh bottom oxide layer 28 in FIG. 7 of Leobandung et al. is etehed to form a smaller treneh whieh is then filled with an oxide (see also column 5, line 20-31). Leobandung et al. are silent claimed dummy pattern in the device region near the boundary.

Therefore, in view of these substantial deficiencies, it is respectfully submitted that Leobandung et al. clearly differ from claimed structure and in no way anticipates the structure stated in amended Claim 1.

Chen et al. diselose a method of fabricating a CMOS deviees on a mixed bulk and SOI substrate, but provides no disclosure of the claimed first isolation formed in the bulk device region so as to separate the bulk device. FIG. 1D of Chen et al. shows shallow trench isolation (STIs) 104 used as local isolation areas placed as the CMOS device isolations in the region labeled "logic, high speed circuits for CMOS/SOI " (see column 3, line 53-58). However, Chen et al. fails to show the claimed first isolation.

Therefore, it is respectfully submitted that Chen et al. clearly differ from claimed structure and in no way anticipates the structure stated in amended Claim 1.

Accordingly, it is respectfully submitted that the outstanding grounds for rejection of Claims 1-4, 6, 10-13 under 35 U.S.C. §102(a) as being anticipated by Leobandung et al. and Chen et al. have been overcome, and it is respectfully requested that these grounds for rejection be withdrawn.

Sato et al. disclose a transistor on capacitor cell having a trench for a DRAM (see column 1, line 21- column 2, line 2). However, Sato et al. like Leobandung et al. are silent about claimed first and second isolations. Thus Sato et al. fail to cure the deficiencies of Leobandung et al. and it is respectfully submitted that the combined teachings of these references in no way render Claim 15 unpatentable.

Consequently, in view of the present amendment and in light of the above comments, it is respectfully submitted that each ground for objection and rejection has been overcome and that the pending claims as submitted herewith are in condition for allowance. An early and favorable action to that effect is therefore requested.

Respectfully submitted,

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